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Design of Hybrid on-Chip Network with Efficient Speed and Low Area

Ms. Sanapala Chitra Prasanna[1], Mrs.Y.P.M. Surya Kiran[2], Mr. Manas Ranjan Biswal[3]
[1]M.Tech Student, Department of Electronics and Communication Engineering, Sanketika Vidya Parishad Engineering College, P.M. Palem, Visakhapatnam-530041
[2,3]Assistant professor, Department of Electronics and Communication Engineering, Sanketika Vidya Parishad Engineering College, P.M. Palem, Visakhapatnam-530041
Email: *chitraprasanna35@gmail.com, ypm.suryakiran20@gmail.com, manas2009muna@gmail.com*

Abstract: Network-on-chip (NoC) has emerged as a vital factor that determines the performance and power consumption of many-core systems. This paper proposes a hybrid scheme for NoCs, which aims at obtaining low latency and low power consumption. In the presented hybrid scheme, a novel switching mechanism, called virtual circuit switching, is proposed to intermingle with circuit switching and packet switching. Flits traveling in virtual circuit switching can traverse the router with only one stage. In addition, multiple virtual circuit-switched (VCS) connections are allowed to share a common physical channel.Moreover, a path allocation algorithm is proposed in this paper to determine VCS connections and circuit-switched connections on a mesh-connected NoC, such that both communication latency and power are optimized. A set of synthetic and real traffic workloads are exploited to evaluate the effectiveness of the proposed hybrid scheme. The experimental results show that our proposed hybrid scheme can efficiently reduce the communication latency and power. For instance, for real traffic workloads, an average of 20.3% latency reduction and 33.2% power saving can be obtained when compared with the baseline NoC.

***Index Terms*:-**NoC , Latency, virtual circuit.

Introduction

WITH the rapid development of advanced nanometer IC technology, continuously shrinking transistor dimensions allow designers to integrate an increasing number of processors or IP cores into a single chip. Traditional bus-based communication is no longer suitable due to its poor scalability. Instead, network-on-chip (NoC) has emerged as a scalable and promising solution to global communications within large multicore systems. Typical examples are the 48-core SCC processor, the 64-core Tile64 chip multiprocessor , and the 80-core TeraFLOPS research chip. All these examples exploit packet-switched (PS) NoCs, which bring the advantage of high flexibility and high bandwidth to communications.

However, such merit is achieved by exploiting a complex router pipeline. The pipeline stages of a baseline PS router include the buffer write (BW) stage, the route computation (RC) stage, the virtual channel allocation (VA) stage, the switch allocation (SA) stage, and the switch traversal (ST) stage. On the one hand, the complex router pipeline leads to a high latency ratio. Although look ahead routing and aggressive speculation shorten the critical path through the router stages, the PS router still occupies a high ratio of communication latency when compared with one-cycle link delay in a mesh-connected NoC. On the other hand, the complex router pipeline leads to a high power ratio. For example, the power of routers can account for 83% of the total communication power in TeraFLOPS, while the power of links only accounts for 17%.

In comparison with PS NoC, circuit switching can significantly lower the communication latency and power consumption, because routing and arbitration are not needed once circuits are set up. Only the ST stage is required on the circuit-switched (CS) connection when a flit traverses a node. However, circuit switching lacks flexibility. If several communications compete for a common physical channel, circuits will be set up in turn. Then, the long setup time will decrease the overall NoC performance.

To address the problems of packet switching and circuit switching, the hybrid scheme that combines packet switching and circuit switching is proposed. It not only can provide high flexibility for communications but also optimize latency of NoCs by establishing CS connections between communication pairs. It had been also demonstrated that establishing CS connections on the PS network can reduce communication power . Moreover, before circuits have been established, packets are transmitted on PS

connections to offset the long setup delay of circuits. However, the fact that CS connections are not allowed to share a common physical channel restricts the number of CS connections. If several packet transmissions will compete for a common physical channel, only one packet transmission can be executed in circuit switching and other packets must travel on PS connections. For the traffic with light congestion, most of communications can be addressed through circuit switching. However, for the traffic with heavy congestion, a very low ratio of CS connections to communications may be incurred, which limits the optimization of latency and power for NoCs.

This paper focuses on further reducing the communication latency and power consumption of NoCs, because the communication latency of NoCs directly influences the data access latency in many-core systems, and the power consumption of NoCs accounts for a high ratio of the total power consumption of the whole chip. In this paper, we propose a novel hybrid scheme, in which a novel switching mechanism, called virtual circuit switching, is first introduced to intermingle with circuit switching and packet switching. In virtual circuit switching, virtual channels (VCs) are exploited to form a number of virtual CS (VCS) connections by storing the interconnect information in routers. Flits can directly traverse the router with only the ST stage. The main advantage of virtual circuit switching is that it can have the similar router pipeline with circuit switching, and can have multiple VCS connections to share a common physical channel. To support the proposed hybrid scheme, one modified router architecture is implemented based on the baseline with a tolerable overhead, and the corresponding switching mechanism is presented in this paper. Based on virtual circuit switching, a path allocation algorithm is proposed to determine VCS connections and CS connections on a mesh-connected NoC under a given network traffic, so that both communication latency and power consumption are optimized. A set of synthetic traffic workloads and real traffic workloads are exploited to evaluate the effectiveness of the proposed hybrid scheme. The experimental results show that our proposed hybrid scheme can efficiently reduce both the communication latency and power consumption. In summary, main contributions of this paper are listed as follows.

1. Virtual circuit switching is first introduced in this paper, and the modified router architecture and its corresponding switching mechanism are presented to support the proposed hybrid scheme.
2. Based on virtual circuit switching, this paper proposes a path allocation algorithm to optimize both communication latency and power consumption.
3. The effectiveness of the proposed hybrid scheme is demonstrated by comparing with the baseline packed switched NoC and VIP design using a set of synthetic and real traffic workloads.

Virtual circuit switching is a process of establishing a temporal connection between two logical links for a duration of a communication session. This operation allows intermediate nodes to set up a temporary path between two nodes, which are communicating with each other. If these two logical links are reserved during a communication session, a virtual circuit dedicated to this particular communication session is established. This approach enables a network to provide a more predictable and stable service because the quality of the communicating channel is obtained prior to the start of the communication session.

In a packet switching network using virtual circuit switching, a particular link must be established from a given source to the destination before any packet is sent. To set up a preplanned link for a communication session, a call setup phase is required, and it causes a delay before a node can send the first packet. In virtual circuit switching, packets can only travel following a single path. This technique ensures that the arrival packets are received in the same order as their original one.

Proposed Work

The basic principle of the proposed hybrid scheme is that VCs are exploited in virtual circuit switching to form a number of VCS connections and multiple VCS connections can share a common physical channel. In this hybrid scheme, VCS connections cooperate with PS connections and CS connections to transmit packets. It is shown in Fig. 1. Fig. 1(a) shows an example of traffic, in which physical channels (1, 2), (7, 11), and (8, 4) are shared by more than one communication, respectively. *(x, y)* denotes the physical channel from node *x* to node *y*. Fig. 1(b) shows CS connections and PS connections after using the conventional hybrid scheme. A CS connection is

configured by recording in each router which input port should be connected to which output port. It is composed of physical channels and routers. However, routers on a PS connection are configured during the (BW, RC, VA, and SA) stages when flits require passing through. A physical channel can be shared by one CS connection and multiple PS connections. Once flits on CS connections arrive at routers, crossbar switches are immediately configured so that the CS flits can bypass directly to the ST stage [4]–[6]. When there is no CS flit, the corresponding ports of crossbar switches are released to PS connections. Fig. 1(c) shows VCS, CS, and PS connections of the proposed hybrid scheme. A VCS connection comprises VCs and routers that have been configured by recording in each router which input VC should be connected to which downstream VC. Crossbar switches of routers are preconfigured during the SA stage before VCS flits require passing through. Because VCS connections are established over VCs, a physical channel can be shared by *n* VCS connections at most (*n* is equal to the VC number). Other communications competing for that physical channel must be executed in packet switching, such as the communication from node 8 to node 4 in Fig. 1.

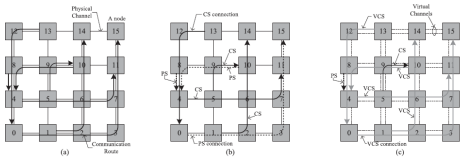

Fig-1: Proposed Hybrid Scheme

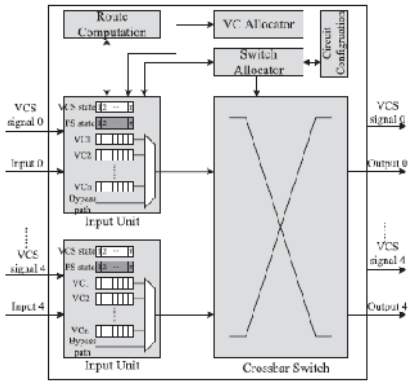

Fig-2: Router Architechture

Third, the circuit configuration unit is to store the interconnect information for CS connections. In this paper, both the PS and the VCS states have *n* fields corresponding to *n* VCs. In addition, these *n* VCs are shared by VCS connections and PS connections. Information of the VC in the downstream router is stored in the VCS state to denote which downstream VC is connected to the corresponding VC. Incoming flits can directly traverse the crossbar switch according to the corresponding field of VCS state. The VCS signal is used to pre-configure the crossbar switch for VCS connections. It can be transmitted simultaneously with the transmission of flits. The VCS signal is *(*log2 *n* + 1*)*-bit wide, including a VC identifier and a flag for representing its validity. The VCS signal does not traverse the crossbar switch, but is generated by the router. It is output when the crossbar switch just completes the configuration for the VCS connection during the SA stage. The overhead caused by VCS signal can be negligible. First, the VCS signal is only issued when crossbar switches of the VCS connection wait to be preconfigured. Due to the low activity of VCS signal, the power overhead caused by VCS signal can be much less than the power saving by bypassing buffer writing, routing, and arbitration of routers. Second, in the network with two VCs, the width of VCS signal is 2 bits.

Compared with the 1-mm flit channel and the 128-bit router, the increased area is less than 1.5% under the estimation of Orion [2]. Moreover, the proposed router architecture has been implemented in Verilog HDL. The synthesis result shows that the modified architecture increases the area by 1.34% without incurring any additional latency on the critical path, when compared with the baseline PS router. As for the data overhead, since route information can be stored in the VCS state and circuit configuration, packets on VCS and CS connections do not need route information. However, packets on PS connections need route information in the data of head flit.

RESULTS

In this project we have studied about the new low area approach of the design is done. Results of which are shown in Figure 4, Figure 5 & Figure 6.

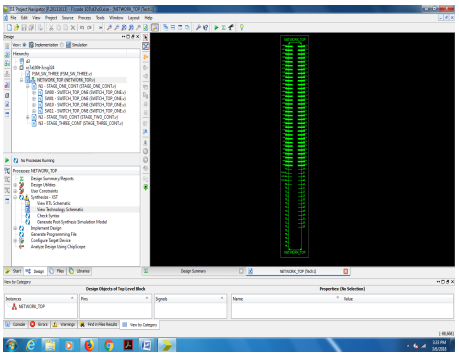

Fig-4:RTL schematic of hybrid scheme

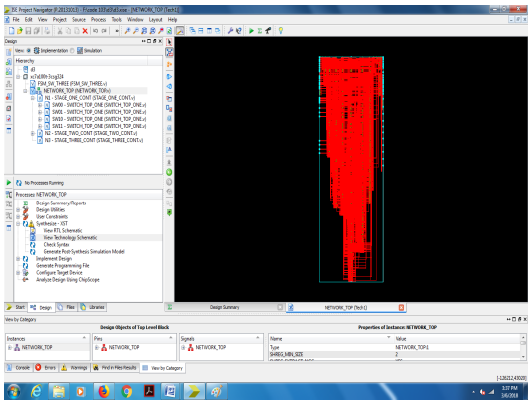

Fig-5: Area report of block

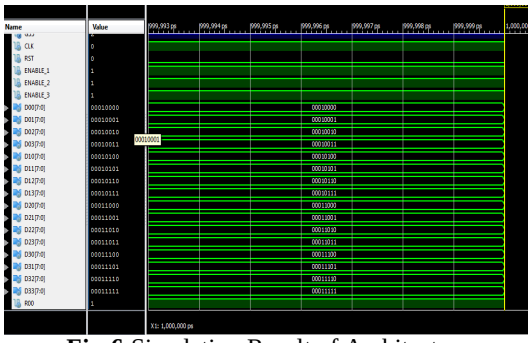

Fig-6: Simulation Result of Architecture.

Summary and Conclusion

In this paper, we present a novel hybrid scheme basedon virtual circuit switching to further reduce communication latency and power of NoCs. The basic principle of the proposed hybrid scheme is to intermingle virtual circuit switching with circuit switching and packet switching. Intermediate router pipelines are bypassed by establishing VCS connections and CS connections. A path allocation algorithm is alsopresented to smartly allocate VCS connections and CS connectionsfor a given traffic in mesh-connected NoCs, such thatthe average packet latency and energy consumption are bothoptimized. To demonstrate the effectiveness of the proposedhybrid scheme, a set of synthetic traffic workloads and realtraffic loads are exploited for evaluation. The experimentalresults show that, compared with the baseline PS NoC withthree-stage routers and the hybrid NoC with VIP connections, our proposed hybrid scheme can obtain further considerable reductions in latency and power consumption.Our future work will focus on extending the current workto support applications with unpredictable communication patterns.Other extensions include the fault tolerance, the qualityof-service (QoS) operation, the multicast delivery service,and the mapping, scheduling of applications based on virtualcircuit switching. In fact, due to the small area overhead,the proposed hybrid scheme can have the similar reliabilityand bit-error rate when compared with the baseline NoCand VIP design. In addition, some fault-tolerance techniques,such as error control codes, structural redundancy, and packetretransmission, can be utilized to increase the reliability ofthe proposed hybrid scheme. Moreover, the proposed hybridscheme can be exploited to achieve the QoS operation. Forexample, VCS connections and CS connections can be limitedto the class of communications that need guaranteed latency,and packet switching can be used to serve the best effort traffic.

A comparison is drawn between the mesh and torus topology as the network on chip are fast developing architecture with a most of the flaws and faults because of the delay and power consumption. The incorporation of Network on Chip through reconfigurable design is another advantage where it can targeted to all portable devices. So, in this paper a different network topology is implemented for advanced Network on Chips.

References

[1] T. G. Mattson *et al*., "The 48-core SCC processor: The programmer'sview," in *Proc. High Performance Computing, Networking, SC*, 2010,pp. 1–11.

[2] S. Bell *et al.*, "TILE64 processor: A 64-core SoC with mesh interconnect,"in*Proc. ISSCC*, 2008, pp. 88–598.

[3] S. R. Vangal*et al.*, "An 80-tile sub-100-W tera FLOPS processor in65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 1,pp. 29–41, Jan. 2008.

[4] N. E. Jerger, L.-S.Peh, and M. H. Lipasti, "Circuit-switched coherence,"in*Proc. ACM/IEEE Int. NOCS*, 2008, pp. 193–202.

[5] A. Abousamra, A. K. Jones, and R. Melhem, "Codesign of NoCandcache organization for reducing access latency in chip multiprocessor,"*IEEE Trans. Parallel Distrib. Syst.*, vol. 23, no. 6, pp. 1038–1046,Jun. 2012.

[6] M. Modarressi, A. Tavakkol, and H. Sarbazi-Azad, "Virtual point-to point connections for NoCs," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 29, no. 6, pp. 855–868, Jun. 2010.

[7] W. Dally and B. Towles, "Route packets, not wires: On-chip interconnection networks," in *Proc. DAC*, 2001, pp. 684–689.

[8] L. Benini and G. D. Micheli, "Networks on chips: A new SoCparadigm,"*IEEE Trans. Comput.*, vol. 35, no. 1, pp. 70–78, Jan. 2002.

[9] U. Y. Ogras and R. Marculescu, "Energy- and performance-driven customized architecture synthesis using a decomposition approach," in*Proc. DATE*, 2005, pp. 352–357.

[10] A. Pinto et al., "Efficient synthesis of networks on chip," in Proc. ICCD,2003, pp. 146–150.

[11] U. Y. Ogras and R. Marculescu, "It's a small world after all: NoCperformance optimization via long-range link insertion," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 7, pp. 693–706,Jul. 2006.