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Design Based on FIFO Buffers with Low power and Speed

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ABSTRACT: This paper proposes an on-line transparent test technique for detection of latent hard faults which develop in first input first output buffers of routers during field operation of NoC. The technique involves repeating tests periodically to prevent accumulation of faults. A prototype implementation of the proposed test algorithm has been integrated into the router-channel interface and on-line test has been performed with synthetic self-similar data traffic. The performance of the NoC after addition of the test circuit has been investigated in terms of throughput while the area overhead has been studied by synthesizing the test hardware. In addition, an on-line test technique for the routing logic has been proposed which considers utilizing the header flits of the data traffic movement in transporting the test patterns.

Keywords: *FIFO Buffers, In-Field Test, NOC, Permanent Fault, Transparent Test*

Introduction

FIFO buffers in NOC infrastructure are large in number and spread all over the chip. Accordingly, probability of faults is significantly higher for the buffers compared with other components of the router. Both online and offline test techniques have been proposed for test of FIFO buffers in NOC. The proposal in is an offline test technique (suitable for the detection of manufacturing fault in FIFO buffers) that proposes a shared BIST controller for FIFO buffers. Online test techniques for the detection of faults in FIFO buffers of NOC routers have been proposed in. However, the technique considers standard cell-based FIFO buffers, while we consider SRAM-based FIFO designs. Thus, faults considered in this brief are different from those targeted in.

Proposed Architecture

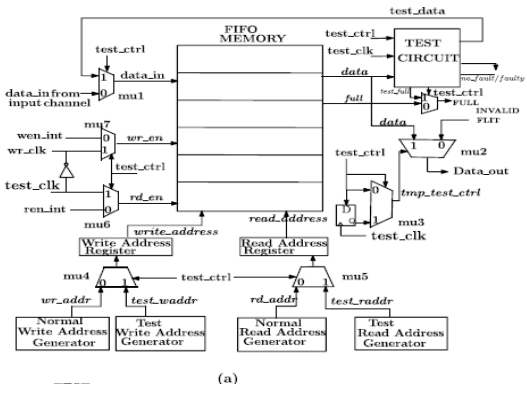
Over the last decade, network-on-chip (NOC) has emerged as a better communication infrastructure compared with bus-based communication network for complex chip designs overcoming the difficulties related to bandwidth, signal integrity, and power dissipation However, like all other systems-on-a-chip (SOCs), NOC-based SOCs must also be tested for defects. Testing the elements of the NOC infrastructure involves testing routers and inter router links.

Significant amount of area of the NOC data transport medium is occupied by routers, which is predominantly occupied by FIFO buffers and routing logic. Accordingly, the probabilities of run-time faults or defects occurring in buffers and logic are significantly higher compared with the other components of the NOC. Thus, test process for the NOC infrastructure must begin with test of buffers and routing logic of the routers. In addition, the test must be performed periodically to ensure that no fault gets accumulated.

The occasional run-time functional faults have been one of the major concerns during testing of deeply scaled CMOS-based memories. These faults are a result of physical effects, such as environmental

susceptibility, aging, and low supply voltage and hence are *intermittent* (nonpermanent indicating device damage or malfunction)in nature. However, these *intermittent* faults usually exhibit a relatively high occurrence rate and eventually tend to become permanent. Moreover, wear-out of memories also cause intermit-tent faults to become frequent enough to be classified as permanent. Thus, there is a need for online test techniques that can detect the run-time faults, which are intermittent in nature but gradually become permanent over time.

Application of SOA-MATS++ test to the FIFO involves writing patterns into the FIFO memory and reading them back. As a result, the memory contents are destroyed. However, online memory test techniques require the restoration of the memory contents after test. Thus, researchers have modified the March tests to transparent March test so that tests can be performed without the requirement of external data background and the memory contents can be restored after test. We have thus transformed the SOA-MATS++ test to trans-parent SOA-MATS++ (TSOA-MATS++) test that can be applied for online test of FIFO buffers. The transparent SOA-MATS++ test generated is represented as {↑*(r x, wx*¯*,r x*¯*, wx,r x)*}



.**Fig-1**:- Hardware implementation of the test process for the FIFO buffers

Results

Simulation results show that periodic testing of FIFO buffers do not have much effect on the overall throughput of the NoC except when buffers are tested too frequently. We have also proposed an online test technique for the routing logic that is performed simultaneously with the test of buffers and involves utilization of the unused fields of the header flits of the incoming data packets

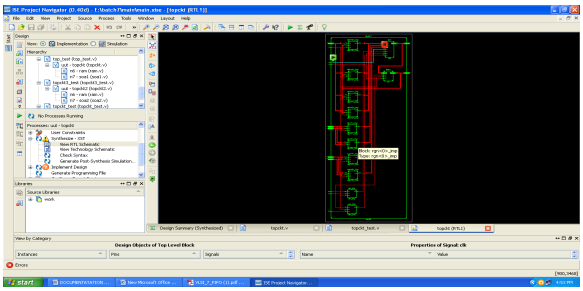


Fig-2:- RTL schematic top module

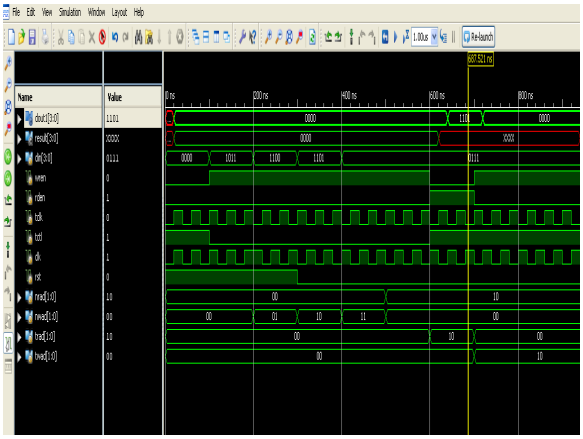


Fig-3:-Simulation design.

Summary and Conclusion

In this paper, we have proposed transparent SOA-MATS++test generation algorithm that can detect run-time permanent faults developed in SRAM-based FIFO memories. The proposed transparent test is utilized to perform online and periodic test of FIFO memory present within the routers of the NoC. Periodic testing of buffers prevents accumulation of faults and also allows test of each location of the

buffer. Simulation results show that periodic testing of FIFO buffers do not have much effect on the overall throughput of the NoCexcept when buffers are tested too frequently. We have also proposedan online test technique for the routing logic that is performed simultaneously with the test of buffers and involves utilization of the unused fields of the header flits of the incoming data packets. Test algorithm and RAM was designed by the Verilog HDL synthesized in Xilinx ISE13.1.

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